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Methods and Approaches to Reduce Development Time and Validation Effort During Physical Prototype Preparation

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ABSTRACT

Physical prototyping remains an indispensable stage of engineering development because it provides direct evidence of product functionality, manufacturability, and reliability. However, repeated prototype iterations are among the dominant contributors to long development cycles, increased costs, and delayed validation readiness. This paper presents an extended review of methods and approaches that reduce development time and validation effort when preparing physical prototypes. Key strategies include front-loaded digital validation, model-based design with software- and hardware-in-the-loop testing, design for manufacturing and assembly (DFMA), additive manufacturing-enabled rapid prototyping, statistically efficient validation planning through design of experiments, and accelerated reliability learning. A structured workflow is proposed to reduce both the number and duration of prototype loops while maximizing learning per iteration.

Keywords: physical prototyping, validation acceleration, DFMA, additive manufacturing, digital validation, HIL testing, design of experiments, reliability learning.

INTRODUCTION

Physical prototypes continue to play a central role in engineering product development. Despite advances in simulation and digital design, prototypes remain essential for validating real-world performance under manufacturing variability, operational loads, and uncertain integration effects.

However, prototype preparation is frequently the slowest and costlier phase of development due to:

- long lead times for tooling and manufacturing;
- repeated redesign cycles after late failure detection;
- insufficiently structured validation planning;
- integration issues between mechanical, electrical, and software sub-systems; and

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- slow reliability learning, often detected late in life-cycle.

Recent studies emphasize validation bottlenecks' dominance over development schedule, enabling approaches shifting validation earlier through digital methods and reducing dependence on repeated physical loops [1].

Simultaneously, additive manufacturing, DFMA methodologies, and model-based verification have enabled faster prototype cycles and improved learning efficiency [2, 3].

This paper investigates the primary methods that reduce development time and validation effort during physical prototype preparation and proposes a structured workflow integrating these approaches into an unified acceleration strategy.

EXPERIMENTAL

Following paper is based on an extended synthesis of peer-reviewed manufacturing and product development research. Journal publications were selected exclusively, focusing on:

- digital validation and twin-based development acceleration [1];
- hardware-in-the-loop testing and embedded system verification [4];
- DFMA-driven reduction of redesign cycles [2];
- additive manufacturing for rapid prototype iteration [3];
- design of experiments for validation efficiency [5];
- accelerated reliability learning methods [6];

Following methods were classified according to their primary time-saving mechanism:

- reducing physical prototype loops' number;
- reducing each prototype iteration duration;
- increasing validation learning per experiment.

Based on this classification, an integrated workflow suitable for JSEE submission was synthesized.

RESULTS AND DISCUSSION

Key methods for prototype development acceleration digital validation and front-loaded testing

Digital validation aims to reduce the number of physical iterations by detecting failures early through virtual evidence. Zhu et al. demonstrate that digital twin-driven validation enables rapid development by shifting key validation activities to the digital domain [1].

Front-loaded validation provides:

- early feasibility confirmation;
- reduced late-stage redesign;
- more efficient prototype planning.

Model-based design and hardware-in-the-loop validation

For embedded and mechatronic products, many failures emerge from controller-plant interaction rather than isolated mechanical weaknesses. Hardware-in-the-loop testing enables verification of control software under realistic operating conditions without waiting for a complete prototype assembly (Table 1).

HIL methodologies provide improved fault coverage and reduce integration time significantly [4].

Design for manufacturing and assembly (DFMA)

DFMA reduces manufacturability-driven redesign by simplifying part structures, providing assembly complexity, and lowering production variability.

Research confirms that early DFMA integration reduces prototype re-spin frequency and shortens development cycles [2].

Additive manufacturing-based rapid prototyping

Additive manufacturing supports rapid production of prototypes, fixtures, and functional test components. This reduces lead time per loop and enables earlier integration testing.

Minguella-Canela et al. highlight the strong

impact of AM prototyping on accelerating product development cycles, especially in early-stage iteration [3].

Statistical efficiency through design of experiments (DOE)

Validation often suffers from inefficient test execution: too many runs with insufficient structured learning. DOE provides an optimal framework for maximizing information per experiment.

Montgomery emphasizes DOE as a critical engineering tool for reducing experimental burden while increasing statistical confidence [5].

Accelerated reliability learning

Reliability weaknesses discovered late in qualification testing are among the most expensive causes of schedule delay. Accelerated life testing (ALT) enables early failure-mode discovery.

Meeker and Escobar demonstrate that accelerated testing is essential for early reliability evidence and reduced late-stage redesign [6].

Integrated workflow for faster prototype validation

The proposed workflow combines these approaches into a coherent development acceleration process:

- Requirements-driven validation planning;
- Digital validation for early defect elimination;
- Model-based SIL/HIL testing for embedded subsystems;
- DFMA-driven prototype-friendly architecture;
- Rapid additive manufacturing iterations;
- DOE-based efficient validation execution;
- Accelerated reliability learning before qualification.

Illustrations of integrated framework for reducing prototype development time by combining digital validation, rapid prototyping, efficient testing, and accelerated reliability learning (Fig. 1).

Above results confirm development acceleration achievement through three dominant pathways:

Table 1. Methods and their time-reduction mechanisms.

Method	Primary time benefit	Key validation output
Digital validation	Fewer prototype loops	Early feasibility evidence [1]
HIL testing	Faster integration cycles	Control robustness proof [4]
DFMA	Reduced redesign frequency	Manufacturability readiness [2]
AM prototyping	Shorter iteration duration	Fit/form/function prototypes [3]
DOE validation	More learning per run	Statistical confidence [5]
Accelerated testing	Earlier weakness discovery	Reliability margins [6]

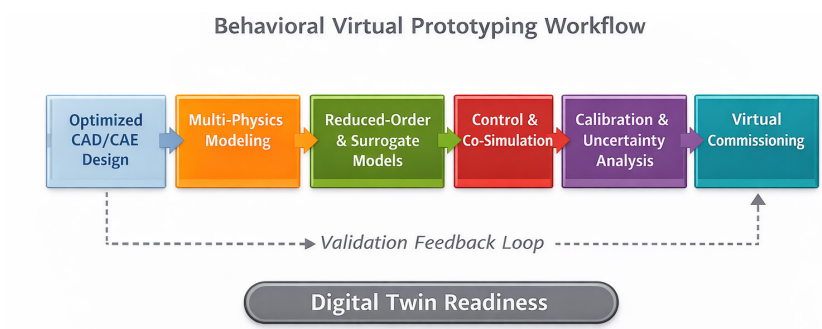

Fig. 1. Prototype development acceleration framework.

Reducing prototype loop count

Digital validation reduces repeated physical builds need by eliminating major design weaknesses early [1]. DFMA further reduces redesign loops caused by manufacturing infeasibility [2].

Compressing loop duration

Additive manufacturing shortens build lead time dramatically, enabling faster feedback and rapid functional testing [3].

Increasing learning efficiency per loop

HIL testing increases range of operational scenarios tested before full assembly availability [4]. DOE maximizes information gained per experiment, reducing total test runs [5].

Accelerated reliability learning prevents costly late-stage failures by exposing weaknesses early [6].

Implementation challenges

Common pitfalls include:

- requirement-linked validation criteria lack;
- AM prototypes misuse missing considering production material differences;
- excessive ad-hoc testing instead of structured DOE planning;
- insufficient calibration between digital validation models and physical evidence.

Future work should integrate AI-assisted validation planning and automated digital evidence pipelines for certification-ready prototyping workflows.

CONCLUSIONS

Reducing development time and validation effort during physical prototype preparation requires an integrated combination of digital validation, embedded system HIL testing, DFMA, additive manufacturing-enabled rapid iteration, DOE-based validation efficiency, and accelerated reliability learning.

Digital twin-driven validation shifts defect discovery earlier [1], while additive manufacturing compresses iteration lead time [3]. DOE increases validation learning efficiency [5], and accelerated testing reduces late-stage redesign risk by exposing reliability weaknesses early [6]. Combined, these methods enable faster convergence to validated product readiness with fewer prototype cycles.

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REFERENCES

1. X. Zhu, Y. Liu, R. Zhao, Toward digital validation for rapid product development based on digital twin, Int. J. Adv. Manuf. Technol. , 117, 2021, 1-18.
2. J.A. Dalgarno, D. Stewart, Design for manufacture and assembly in product development: Reducing redesign cycles, Journal of Manufacturing Systems, 37, 2015, 15-228.
3. J. Minguella-Canela, A. Mueller, P. Gembarski, Additive manufacturing for rapid prototyping and its impact on product development time, Rapid Prototyping Journal, 26, 4, 2020, 623-635.
4. S.V. Abeykoon, J. Kelly, R. Gosine, Hardware-in-the-loop testing for embedded mechatronic validation: A review, Robotics and Computer-Integrated Manufacturing, 68, 2021.
5. D.C. Montgomery, "Design of experiments for product and process validation," Quality Engineering, 31, 2, 2019,181-195.
6. W.Q. Meeker, L.A. Escobar, Accelerated life testing and reliability evidence in product development," Technometrics, 60, 3, 2018, 243-259.